ABSTRACT OF THE DISCLOSURE

The invention relates to a RAM store having a shared SA structure, in which sense amplifiers (SA) arranged in SA strips (10) between two respective adjacent cell blocks are used by a plurality of bit line pairs (21, 22; 21-24) from the adjacent cell blocks and the bit line pairs (21, 22; 21-24) have respective charge equalization circuits individually associated with them for the purpose of performing charge equalization between the bit line halves of the bit line pairs (21, 22; 21-24) in a precharge phase, where a shorting transistor (30) is provided which, when prompted by a control signal (EQLx), connects the bit line halves (BLT, BLC) of the bit line pairs (21, 22; 21-24) which are in the precharge phase to one another. The shorting transistor (30) is arranged in or on the respective sense amplifier (SA) jointly for all bit line pairs (21, 22; 21-24) which can be connected to a respective sense amplifier (SA), and it can be switched by a separate shorting control signal (EQLx) via a dedicated control line (9).